A Re-Configurable Receiver Architecture for 3G Mobiles

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Abstract — A re-configurable, highly-integrated receiver architecture is described for use in 3rd-generation mobile handsets. It is intended for dual-mode UMTS and GSM operation but should be capable of operating in other modes such as CDMA2000. The receiver achieves its adaptability by using a single down-conversion approach to either a zero IF or a near-zero IF and then digitizing as much of the IF signal chain as possible. Notwithstanding its re-configurability, system simulations indicate that the receiver should achieve state-of-the-art performance.

I. INTRODUCTION

As the deployment of 3rd-generation (3G) cellular communication systems gathers pace, the need for lower-cost, re-configurable handset products that can operate in several different modes becomes increasingly important. Some of the earliest 3G products to reach the market will inevitably be based on traditional receiver concepts and will not have the cost/functionality profile needed for the
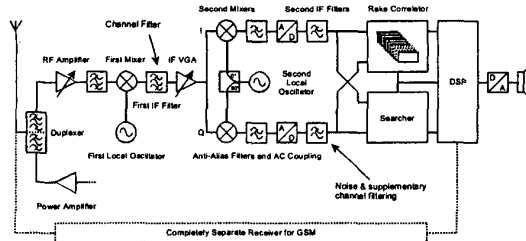

Fig. 1. A conventional dual-mode approach

longer term. Hence, new receiver architectures are required, one possible proposal for which is the subject of this paper. The particular standards that will be addressed are the FDD (Frequency-Division Duplex) version of UMTS (Universal Mobile Telecommunication System) and the 2nd-generation standard, GSM (Global System for Mobile communications). However, the architecture can be re-configured to operate in other modes such as CDMA2000. The UMTS system is based on wideband code-division multiple access (W-CDMA) and has a signal bandwidth of approximately 4 MHz. The GSM system by contrast, is based on time-division multiple access (TDMA) and its signal bandwidth is only 200 kHz.

After describing a "conventional" approach to the dual-mode receiver problem, the paper will deal with the needs of the UMTS and GSM modes separately. The proposed system configuration will be described for each case, together with a prediction of the likely receiver performance derived by system simulation. The paper will then conclude with an illustration of how the two configurations can be merged together to form a complete dual-mode architecture.

II. A CONVENTIONAL APPROACH

A low-risk approach is shown in Fig. 1 in which the UMTS and GSM modes are processed by separate receiver chains. For the sake of clarity, the figure illustrates only the UMTS receiver part but both chains are based on the dual-conversion superhet. It is well known that this type of receiver offers excellent sensitivity and selectivity. However, its heavy reliance on highly-selective, passive, analogue filters makes it relatively expensive to manufacture and difficult to re-configure for multi-mode operation. It also relies heavily on automatic gain-control (AGC) which is a further impediment to multi-mode operation. Analogue-to-digital conversion (ADC) takes place very late in the receiver chain, leaving most of the signal processing in the analogue domain.

III. UMTS (FDD) CONFIGURATION

Responsibility for the technical specification of UMTS lies with the 3rd-Generation Partnership Project (3GPP) [1] and details of the required performance characteristics of a UMTS receiver can be found in [2]. When the required characteristics are taken into consideration, it becomes clear that a zero-IF architecture [3] is one of the most attractive options, irrespective of the need for re-configurability. In general, the zero-IF architecture offers the important advantage of being able to be integrated onto an IC without the need for expensive, off-chip, IF filters. It does have some disadvantages associated with DC offsets and 2nd-order intermodulation products generated in the front-end mixers which occupy the same frequency band as the wanted signal. These can desensitize the receiver, militating against its use for many narrow-band systems such as GSM. For UMTS however, the problem is not so serious, mainly because of the spread-spectrum nature of the air interface. With such a wide bandwidth, it

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is possible to use AC couplings in the receiver to filter out the DC offsets and some of the other 2nd-order products without significantly degrading sensitivity.

As well as the obvious cost advantages, integrating the channel filters in a zero-IF receiver also leads to improved adaptability. This is true even if the filters in question are still analogue devices. However, the scope for re-configuration is substantially improved if a larger proportion of the signal processing takes place in the digital domain. In the proposed zero-IF receiver
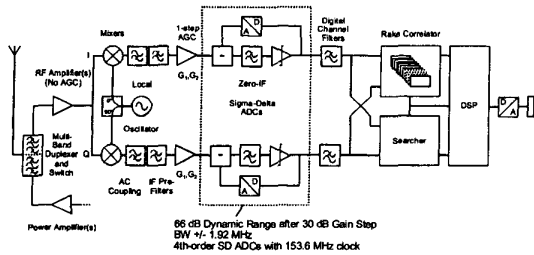

Fig. 2. Proposed UMTS receiver configuration

configuration for UMTS shown in Fig. 2, this is achieved by advancing the position of the ADCs in the signal chain to the point where most of the analogue selectivity and AGC is eliminated. Whilst this makes re-configuration very much easier, it does have the disadvantage of requiring the ADCs to handle a much greater dynamic range of signals. However, by careful choice of the type of ADC and the associated decimation filtering regime, it is possible to avoid any substantial increase in power consumption.

As shown in Fig. 2, not quite all the selectivity has been removed before the ADCs and a little AGC remains. A pair of 1st-order pre-filters with a lowpass cut-off frequency of about 9 MHz attenuate some of the largest blocking interferers at frequency offsets greater than 15 MHz and a pair of very simple AGC elements reduce the total power in the wanted signal bandwidth for the top 30 dB of the dynamic range. They break the basic principle of digitizing the whole of the IF signal chain but they do give a worthwhile reduction in ADC dynamic range and neither is a real impediment to re-configuration. The highpass filters shown in the figure represent simple AC couplings which remove DC offsets in the I and Q components of the IF signal before they reach the ADCs. System simulations have indicated that these will have no adverse effect on receiver sensitivity for cut-off frequencies below 100 kHz.

The ADCs used in the receiver are sigma-delta (SD) modulator types clocked at a frequency of 153.6 MHz (i.e. 40 times the chip rate of 3.84 MHz). Two different

designs have been investigated, one using a 5th-order, time-continuous, loop filter with a 1-bit output comparator and the other using a 4th-order filter with a 1½ bit (i.e. 3-level) output comparator. The time-continuous filters and the high clock speed minimize the need for additional anti-alias filtering. The 4th-order version was tried initially because it was thought to be more tolerant of clock jitter; in fact both designs are able to achieve the dynamic range requirement for UMTS mode of 66 dB in a ±1.92 MHz bandwidth.

Immediately after the ADCs, a pair of digital filters provide the receiver with the bulk of its selectivity. Implemented as FIR (finite impulse response) devices, these remove all incoming interferers as well as the high frequency quantisation noise generated by the ADCs. They have a root-raised-cosine (RRC) characteristic to match the characteristic used in the baseband filter of the basestation transmitter. For maximum power efficiency, it is critical that these filters perform their filtering and decimation tasks in a single step. This exploits the bitstream nature of the output of the ADCs and avoids the need for digital multiplication. Decimation would be by a factor of 10 for a sampling rate at the input to the rake correlator of 15.36 MHz.

Dimensioning the various component parts of the receiver calls for a very careful analysis of the UMTS performance requirement, the details of which are beyond
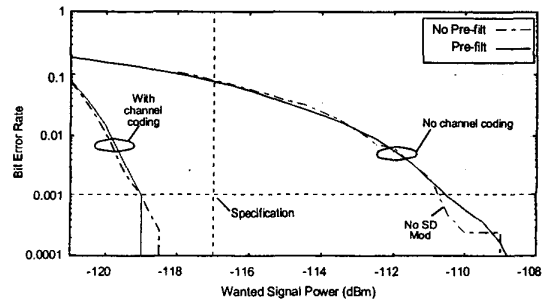

Fig. 3. Sensitivity simulation for UMTS mode

the scope of this paper. However, it may be helpful to state at least the noise figure requirement which is 8.5 dB for a receiver sensitivity of −119.5 dBm. This gives a 2.5 dB margin on the minimum requirement of −117 dBm [2]. The equivalent noise power at the input to the receiver is -99.5 dBm. If all blocking interferers are reduced to a level of −44 dBm by pre-filtering and the quantisation noise generated by the ADCs is equivalent to −110 dBm at the receiver input, this leads to the 66 dB dynamic-range requirement of the two ADCs.

As first evidence of the basic performance capability in UMTS mode, the result of a system simulation is plotted in Fig. 3. The simulation pertains to the 12.2 kb/s data-rate service but also indicates the bit-error-rate (BER) performance without the effects of channel coding. The figure shows that the BER with channel coding reaches the necessary 0.1% at a wanted signal power of –119 dBm. This compares with a figure of –110.5 dBm for the case of no channel coding, indicating that the coding gain is in the order of 8.5 dB. The results also show that neither the analogue pre-filters nor the quantisation noise of the SD modulators has any real impact on performance.

IV. GSM CONFIGURATION

Responsibility for the technical specification of GSM also now lies with 3GPP but details of the required receiver performance can be found in [4]. As a relatively narrow band system based on Gaussian minimum shift key (GMSK) modulation, GSM is not quite so suited to the zero-IF architecture as UMTS. The presence of either DC offsets or a hole caused by AC coupling in the centre of the spectrum will usually cause unacceptable damage to the modulation. Only recently are zero-IF solutions for GSM beginning to appear and these are the result of taking extreme care with the cancellation of DC offsets.

The low-IF or near-zero-IF receiver architecture [5] is a concept that was introduced to overcome the DC-offset problems with the zero-IF architecture. By mixing the
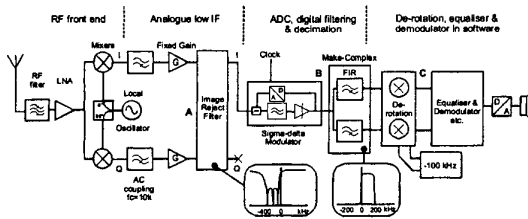

Fig.4. Proposed GSM receiver configuration

wanted signal down to a low IF of half the channel spacing (i.e. 100 kHz for GSM) instead of zero, the hole now caused by AC coupling is moved to the lower side of the signal spectrum where it is very much less damaging. There is the minor complication of requiring a complex channel filter instead of the simple lowpass filters of the zero-IF receiver but the analogue solution described in [5] has been very successful. A low-IF GSM receiver will invariably have a much better performance than a zero-IF type in a hostile interference environment.

With re-configuration in mind, the receiver architecture of Fig. 2 could be made to operate with a low IF for the

GSM mode. However, to avoid a heavy loss in ADC efficiency, this would ideally require the SD modulators to become complex so that the centre of the quantisation noise spectrum could be aligned with the 100 kHz IF. Given the already difficult design objective in meeting the performance requirements for UMTS, the modifications that would be required to make the ADC complex are considered too great a risk. In the proposed receiver configuration shown in Fig. 4, the need for a complex sigma-delta ADC is avoided by a novel variation to the IF signal processing. Instead of processing both the I and Q components of the low-IF output from the front end, the Q
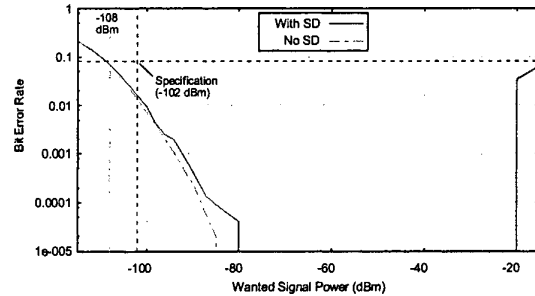

Fig. 5. Sensitivity simulation for GSM mode

component is discarded and only the I component is passed to the SD modulator. The effect of this is to make the spectrum of the now real IF signal symmetrical about zero, as if the IF were itself zero. Hence, the spectrum is naturally aligned with that of the quantisation noise spectrum of the SD modulator. It is then relatively easy to make the IF signal complex once again by performing the equivalent of a Hilbert transform in the digital channel filters that follow. The last step before equalisation and demodulation is to translate the signal to a zero-IF in a digital de-rotation by –100 kHz.

An obvious consequence of processing only the I component of the IF signal is a loss of image rejection. Any interferer present in the lower adjacent channel to the wanted signal will also be folded over about zero and be indistinguishable from the wanted signal. However, this problem is easily overcome by filtering the output of the front-end with a simple passive polyphase filter. Investigations have shown that a 3-stage filter is able to provide the necessary attenuation of about 30 dB over the band –400 kHz to zero. It is necessary to attenuate an interferer in the lower alternate channel as well as the adjacent channel to avoid the tails of its spectrum falling into the band of the wanted signal at a comparatively high level. However, there is no penalty for this and the filter consumes little or no power.

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As in the case of the UMTS mode, the receiver configuration for GSM proposed in Fig. 4 is heavily digitised. It uses no AGC and the polyphase filter should be viewed as only a pre-filter, the vast majority of the channel selectivity being implemented by the FIR filters in the digital domain. The DC offsets from the mixers are removed by AC coupling whose highpass characteristics have a non-critical cut-off frequency in the region of 10 kHz. The use of a single SD modulator ADC results in a very useful saving in power consumption. It is possible to use the same ADC as for the UMTS mode by simply scaling the bandwidth of the loop filter and changing the clock frequency to 26 MHz (i.e. 96 times the bit rate of 270.8333 kb/s). With a 26 MHz clock, the 5th-order, 1-bit modulator achieves the necessary dynamic range, which in the absence of AGC is approximately 100 dB in a ±200 kHz bandwidth. The channel/make-complex filters use the same physical FIR structures used for the UMTS mode but with a different set of coefficients. They decimate directly to the bit rate, and as previously explained, do so in a single stage to minimize power consumption.

Whilst the GSM specification [4] calls for a receiver sensitivity of −102 dBm, the industry standard is now in the region of −108 dBm. To achieve this sensitivity, the latest receivers have a noise figure of 6.5 dB. This is lower than the 8.5 dB requirement for UMTS and hence with only minor modification for the extra IF bandwidth a typical GSM front-end should be able to deal with both modes.

System simulations have been carried out to verify the performance capability of the new receiver configuration for GSM. From the results plotted in Fig. 5, it is clear that the receiver achieves the required 8% BER for a TU50 fading profile at a wanted signal power of −108.5 dBm. This is a good result. There appears to be a negligible loss of sensitivity due to the quantisation noise generated by the SD modulator but the rise in BER at −20 dBm is an indication of a slight shortage of dynamic range. This can be corrected by some minor re-dimensioning or the addition of a small amount of AGC.

V. CONCLUSIONS

If the two receiver configurations of Figs. 2 and 4 are merged, the dual-mode receiver architecture takes on the form shown in Fig. 6. As indicated by the dotted outlines, most of the functional blocks of the receiver are re-used for the different modes. Even some of the baseband processing, shown separately in the figure, could take place on a common DSP core. If the bandwidth of the AC coupling is set to suit GSM and the bandwidth of the pre-

filters set to suit UMTS, then they can be left in situ for both modes. An extra gain step needs to be added to the IF pre-amplifiers for the GSM mode to align the signal dynamic range to that of the SD modulators but this does not constitute any extra AGC. The image reject filter used for GSM should be bypassed in UMTS mode but if it had to be left in place, the impact on performance for UMTS is likely to be small. Both SD modulators are active and clocked at a frequency of 153.6 MHz in UMTS mode,
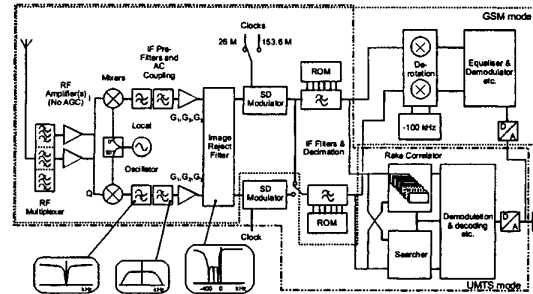

Fig. 6. Dual-mode receiver architecture

each feeding one of the two digital, FIR channel filters. In GSM mode, one of these is shut down, whilst the other is re-configured and clocked at the alternative frequency of 26 MHz. In this case, both digital filters are driven by the single SD modulator.

The receiver described herein, as well as being fully integrated, should offer improved adaptability and re-configuration potential to future generations of mobile equipment. A fundamental principle has been the early digitization of the IF signal chain, eliminating most of the AGC and moving most of the channel filtering into the digital domain. The main parts of the receiver have been dimensioned and its feasibility demonstrated by system simulations. Work is currently in progress to demonstrate its capability in practice.

REFERENCES

[1] http://www.3gpp.org
[2] 3GPP, TSG RAN WG4, "UE Radio Transmission and Reception (FDD)," Release 1999, 3GPP TS25.101, V3.7.0 (2001-06).
[3] B. Razavi, "Design Considerations for Direct-Conversion Receivers," IEEE Trans. On Circuits and Systems-II, Vol. 44, No. 6, June 1997.
[4] ETSI Secretariat, "GSM: Digital Cellular Telecommunications System (phase 2) Radio Transmission and Receptions (GSM 05.05)," ETS 300 577, F-06921 Sophia Anitpolis, Cedex, France, March 1996.
[5] B. J. Minnis, et al, "A Low-IF Polyphase Receiver for GSM Using Log-domain Signal Processing", IEEE RFIC2000 Symposium, Boston MA, June 11-13, 2000, pp83-86.